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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/605,357	09/25/2003	HOUNG-JIE CHANG	11535-US-PA	2356		
31561	7590 04/19/2004		EXAM	EXAMINER		
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE			NOVACEK,	NOVACEK, CHRISTY L		
7 FLOOR-1,	NO. 100 T ROAD, SECTION 2		ART UNIT	PAPER NUMBER		
TAIPEI, 100		2822				
TAIWAN			DATE MAILED: 04/19/200	4		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	// 1				
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Office Action Summary		10/605,357	CHANG ET AL.					
	.u. y	Examin r	Art Unit					
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A SHORTENED STATUTORY PEI THE MAILING DATE OF THIS CO - Extensions of time may be available under the after SIX (6) MONTHS from the mailing date oi - If the period for reply specified above is less th - If NO period for reply is specified above, the m - Failure to reply within the set or extended perion Any reply received by the Office later than thre earned patent term adjustment. See 37 CFR 1	MMUNICATION. provisions of 37 CFR 1.1: f this communication. an thirty (30) days, a reply aximum statutory period v d for reply will, by statute, e months after the mailing	36(a). In no event, however, may a reply be within the statutory minimum of thirty (30) of the cause the application to become ABANDOI	timely filed lays will be considered timely. om the mailing date of this cor NED (35 U.S.C. § 133).					
Status								
1)⊠ Responsive to communication	on(s) filed on 25 Se	eptember 2003.						
2a) ☐ This action is FINAL .		action is non-final.						
3) Since this application is in co	<i>,</i> —		rosecution as to the	merits is				
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Disposition of Claims								
<u> </u>	in the application							
-	 ✓ Claim(s) <u>1-14</u> is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 							
5)⊠ Claim(s) <u>1-3</u> is/are allowed.		With definition and the second						
	Si) ☐ Claim(s) <u>4-14</u> is/are rejected. Claim(s) is/are objected to.							
8) Claim(s) are subject to		r election requirement.						
Application Papers								
9) The specification is objected	to by the Evamine	r						
10)⊠ The drawing(s) filed on <u>25 Se</u>	•		acted to by the Evam	iner				
		drawing(s) be held in abeyance. S	•	iner.				
		ion is required if the drawing(s) is o	` '	R 1 121(d)				
11) The oath or declaration is obj	=		•	, ,				
Priority under 35 U.S.C. § 119	•							
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12) Acknowledgment is made of a a) All b) Some * c) No		priority under 35 U.S.C. § 119(a)-(d) or (f).					
1. ☐ Certified copies of the		s have been received						
	•	s have been received in Applica	stion No					
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application from the In	·	-	ved in this ivational S	nage				
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Attachment(s)			(070.4:0)	•				
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing F 	Review (PTO-948)	4) L Interview Summa Paper No(s)/Mail						
3) Information Disclosure Statement(s) (PTC			Patent Application (PTO-	152)				
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DETAILED ACTION

This office action is in response to the communication filed September 25, 2003.

Claim Objections

Claim 14 is objected to because of the following informalities: in line 1 of the claim, "deviceof" should be separated into "device" and "of". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 2 of claim 4 recites the limitation of "said removing step". However, lines 7-8 of claim 1, upon which claim 4 depends, recites "polishing said semiconductor device until said plug above said gate is removed" and line 10 of claim 1 recites "removing said insulating layer". Therefore, it is unclear as to which of these removing steps "said removing step" recited in claim 4 is referring.

Line 3 of claim 5 recites the limitation of "said etching process". However, line 3 of claim 4, upon which claim 5 depends, recites "a wet etching process" and line 4 of claim 4 recites "a dry etching process". Therefore, it is unclear as to which of these etching processes "said etching process" recited in claim 5 is referring.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Yeh (US 6,709,879).

Regarding claim 8, Yeh discloses a semiconductor device having at least two adjacent conducting layers (202a/202b/202c) and an insulating layer (204) disposed between the conducting layers, a defect (203a/203b) existing between the conducting layers, polishing the semiconductor device to partially expose the conducting layers, removing the insulating layer between the conducting layers and detecting the defect between the conducting layers (Fig. 2B-2E; col. 2, ln. 27 – col. 3, ln. 14).

Claims 8, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Jarvis (US 6,258,437).

Regarding claim 8, Jarvis discloses a semiconductor device having at least two adjacent conducting layers (116) and an insulating layer (118/120/122) disposed between the conducting layers, a defect (128a/128b) existing between the conducting layers, polishing the semiconductor device to partially expose the conducting layers, removing the insulating layer between the conducting layers and detecting the defect between the conducting layers (Fig. 5-10; col. 7, ln. 27 - col. 9, ln. 9).

Regarding claim 12, the removing step is a dry etching process (col. 8, ln. 6-16).

Regarding claim 13, the dry etching process is a reactive ion etching (RIE) process (col. 8, ln. 6-16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarvis (US 6,258,437) in view of Summerfelt et al. (US 20030124791).

Regarding claims 9 and 10, Jarvis discloses that after the polishing step, photoresist material is deposited on the insulating layer. The photoresist is patterned and is used to remove the insulating layer (col. 8, ln. 6-16). Jarvis does not disclose cleaning the semiconductor device after the polishing step and before the removing step. Summerfelt discloses a process of using a photoresist to pattern an underlying layer. Summerfelt states that the photoresist may leave a residue behind when it is removed and it is necessary to remove this residue by a process such a using a deionized water (DI) rinse (para. 128). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a DI rinse and dry to clean the semiconductor device after removing the photoresist layer of Jarvis because the photoresist can leave residue and particles behind after it is removed and it would be beneficial to remove this residue to allow the defects in the device to be more readily seen.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 6,709,879) in view of Jarvis (US 6,258,437).

Regarding claim 11, Yeh discloses that the insulating layer may be silicon nitride and may be removed using phosphoric acid (H₃PO₄) (col. 2, ln. 60-62). Yeh does not specifically disclose that this process is a wet etch. Like Yeh, Jarvis teaches a step of etching silicon nitride using phosphoric acid. Jarvis states that this process is a wet etch (col. 8, ln. 36-50). At the time of the invention, it would have been obvious to one of ordinary skill that the phosphoric etch disclosed by Yeh is to be a wet etch because Jarvis teaches that the process of etching silicon nitride using phosphoric acid is a wet etch.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 6,709,879) in view of Nakasuji et al. (US 6,593,152).

Regarding claim 14, Yeh does not disclose what apparatus is used to examine the semiconductor device for defects. Nakasuji discloses a scanning electron microscope (SEM) device that can be used to detect defects on semiconductor wafers with improved efficiency and accuracy (col. 3, ln. 5-25). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the SEM device of Nakasuji to detect the defects of Yeh because Nakasuji discloses that his SEM can examine a wafer for defects with improved efficiency and accuracy.

Allowable Subject Matter

Claims 1-3 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reasons for the allowance of claims 1-3 is the inclusion therein, in combination as currently claimed, of the limitations of a semiconductor device having a defect between a plug connected to the source/drain and the gate, polishing the device until the plug above the gate is removed, removing an insulating layer between the gate and the plug and detecting the defect. These limitations were found in claims 1-3 and are neither disclosed nor taught by the prior art of record, alone or in combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Li (US 6,168,960) discloses an insulating layer disposed between adjacent conductive lines and polishing the substrate until the conductive lines are exposed and can be examined for defects.

Lee (US 6,107,201) discloses a method of examining a defect in a metal contact of a source/drain region of a semiconductor substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN April 13, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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